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A High-Efficiency MOSFET Transformerless Inverter for Nonisolated Microinverter Applications

Abstract

With worldwide growing demand for electric energy, there has been a great interest in exploring photovoltaic (PV) sources. The PV microinverter has become a popular trend for its great flexibility in system installation and expansion, safety of low-input voltage, and high system-level energy harnessing under shading. Because it is not mandatory for PV microinverters to have galvanic insulation, the nonisolated architecture, is an ideal choice for high efficiency design. Gu *et al*. reported a nonisolated high boost ratio dc–dc converter, which boosts PV panel voltage to around 380 V dc-link voltages for 240 V grid voltage and achieves high efficiency over wide input voltage range. In order to achieve high system efficiency and minimize the system common-mode (CM) voltage, the secondary stage of the nonisolated PV microinverter requires a high efficiency transformerless inverter.

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Existing system

The topology called "Highly Efficient and Reliable Inverter Concept" (HERIC), derives directly from the Full-Bridge converter, in which a bypass leg has been added in the AC side by means of two back-to-back IGBTs operating at grid frequency. The bypass branch has two important functions: decoupling the PV array from The grid (using a method called "AC decoupling"), Avoiding the presence of high-frequency voltage Components across it and preventing the reactive power exchange between the filter inductors and Cin during the zero voltage state, thus increasing efficiency [2]. The converter operates as it follows during the positive half-cycle S+ remains connected, whereas S1 and S4 commutate at switching frequency in order to generate both active and zero vectors. When an active vector is present (S1 and S4 are ON), current flows from the PV panels to the grid, while, when a zero vector occurs, S1 and S4 are switched OFF and the current flows through S+ and D-, this is the freewheeling situation. On the other hand, when the negative cycle is coming, S+ goes OFF and S- goes ON, whereas S3 and S2 commutate at switching frequency. It means that an active vector is present when S3 and S2 are ON, therefore the current flows from the PV panel towards the load, thus when S3 and S2 turn off, a zero voltage

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vector is present in the load, then current flows through S- and D+.

Proposed system

*S*1, *S*2, D1, D2, and *Lo*1 make up one proposed phase leg and *S*3, *S*4, *D*3, *D*4, and *Lo*4 make up another proposed phase leg; *S*5 and *D*5 provide a freewheeling loop for positive current; *S*6 and *D*6 provide a freewheeling loop for negative current. Phase leg splitting inductors *Lo*1 and *Lo*4 can be coupled together and filter inductors *Lo*2 and *Lo*3 can be coupled together. The phase-leg splitting inductors *Lo*1 and *Lo*4 have 50% utilization, but the filter inductors *Lo*2 and *Lo*3 have full utilization. The phase-leg splitting inductors *Lo*1 and *Lo*4 are only designed for *di*/*dt* suppression with a value much smaller than the filter inductance. In this paper, the total inductance of phase-leg splitting inductor is 86 μH, and the filter inductors *Lo*2 and *Lo*3 are 4.7 mH. So even though the phase-leg splitting inductors only have 50% utilization, the overall inductance utilization is over 98%. The proposed inverter almost achieves almost full utilization of magnetics. Thus, the cost and volume of magnetic can almost be reduced by half. In addition, the proposed inverter still does not need PWM dead-time, only has two devices in the conduction loss, and has no risk from reverse recovery of MOSFET body diodes.

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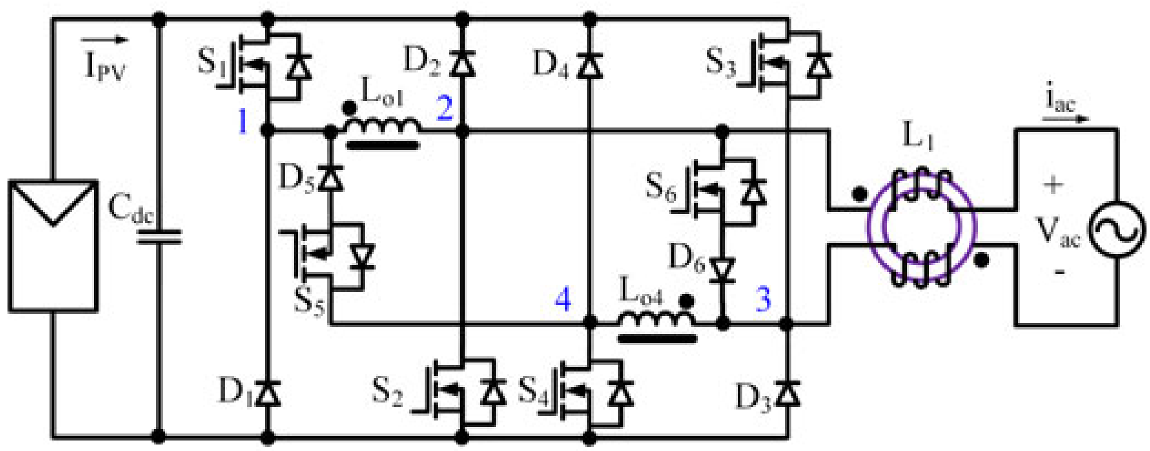

Advantages

- High efficiency
- Low CM voltage
- Improved magnetic utilization

Applications

- Photovoltaic (PV) sources.

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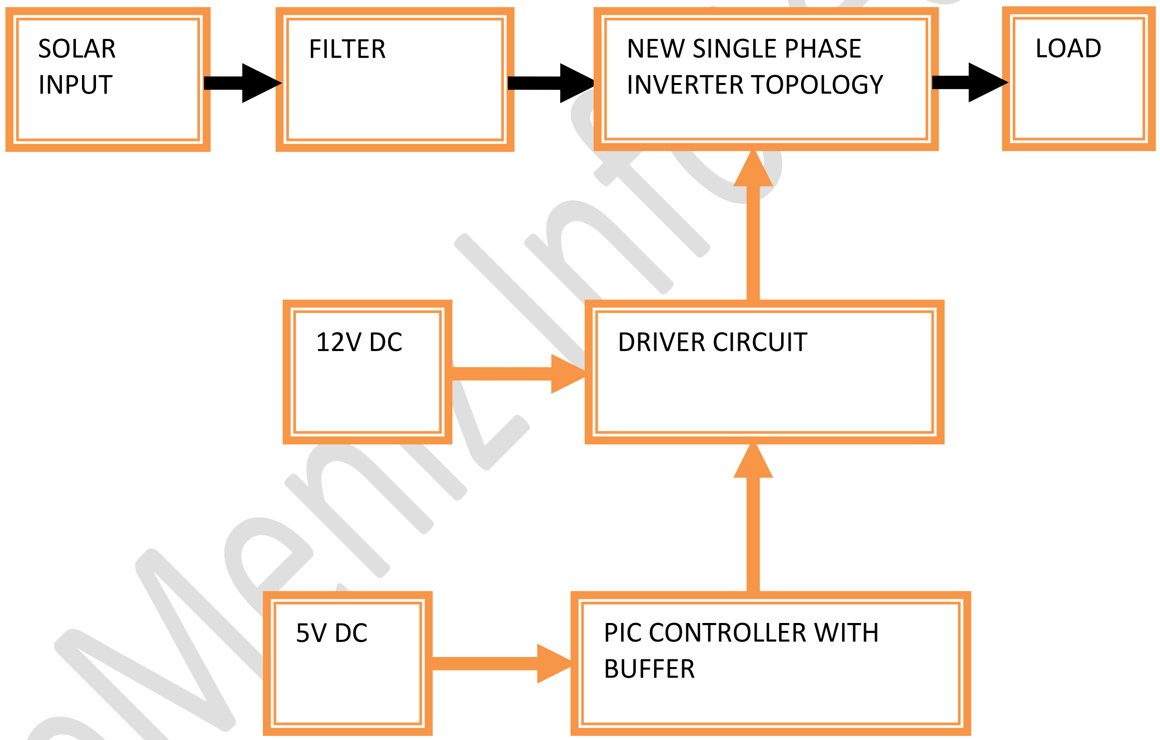
Block diagram



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Tools and software

- MPLAB – microcontroller programming.
- ORCAD – circuit layout.
- MATLAB/Simulink – Simulation.